Listing of the Claims:

Below is a listing of all claims using a strikethrough and underlining to show changes.

1-3. (Canceled)

4. (previously presented) A DLL (delay locked loop) circuit for outputting a phase lock signal having a predetermined phase relationship with an input signal, said DLL circuit comprising:

a functional block having a constant current source; and

a bias generation means for generating a constant current source bias signal for controlling the constant current source of the functional block, said bias generation means comprising bias control means which changes the bias signal according to the frequency of the input signal,

wherein the bias control means comprises:

a control circuit for outputting a first counting control signal which controls the start of counting of the input signal based on a predetermined external signal;

a counting control means for outputting a second counting control signal after the elapse of a predetermined time from the input of the first counting control signal;

counting means for controlling the start and end of counting of the input signal. respectively according to the first counting control signal and the second counting control signal; and

correction signal generation means for outputting a bias correction signal based on the results of counting by the counting means.

5. (original) The DLL circuit according to claim 4, wherein the output signal of the counting control means is controlled by the primary bias signal.

6. (previously presented) The DLL circuit according to claim 4, wherein:

the counting control means comprises PHOS (p-channel MOS), first NMOS (n-channel MOS), second NMOS (n-channel MOS), a capacitive element and a comparison circuit;

a source electrode terminal of PMOS is connected to a power terminal, a drain electrode terminal of PMOS is connected by common connection to a drain electrode terminal of the first NMOS, a first electrode terminal of the capacitive element, and a first input terminal of the comparison circuit;

source electrode terminal of the first NMOS is connected by common connection to d drain electrode terminal of the second KMOS:

a source electrode terminal of the second NMOS, together with a second electrode terminal of the capacitive element, is connected to a ground terminal;

a gate electrode terminal of each of PMOS and the first NMOS is connected by common connection to an output terminal of the control circuit for outputting the first counting control signal; a gate terminal of the second NMOS is connected to a primary bias output terminal of the first bias generation circuit; and

a second input terminal of the comparison circuit is connected to a reference signal terminal having a predetermined potential, and a second counting control signal is output from an output terminal of the comparison circuit

7. (currently amended). A DLL (delay locked loop) circuit for outputting a phase lock signal having a predetermined phase relation ship with an input signal, said DLL circuit, comprising:

a functional block having a current source;

bias generation means for generating a current source bias signal for controlling the current source of the functional block, wherein said bias generation means comprising bias control means which changes the bias signal according to the frequency of the input signal;

a differential amplifier receiving current from the current source;

~~The DLL circuit according to claim 1, further comprising:~~

phase shifting means for generating m phase shift processing signals, wherein m is an integer of two or more, different from each other in phase based on the input signal;

phase comparison means which compares the phase of the input signal with the phase of the phase lock signal to detect a phase difference and, based on the detected phase difference, outputs a phase control signal;

phase synthesizing means for outputting a phase corrected signal having a predetermined phase relationship with the input signal based on the m phase shift processing signals, produced by the phase shifting means, and the phase control signal; and

first duty correction means which corrects the duty of the phase corrected signal and outputs the phase lock signal.

8. (original) The DLL circuit according to claim 7 further comprising second duty correction means for correcting the duty of the input signal and outputting a duty corrected signal, wherein the duty corrected signal is input into the phase shifting means.